Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	393	257/391.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/01/09 10:41
S1	1	(clock adj synchronous) and (rising with edge with flank) and (clock adj buffer) and inverter	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/01/09 10:41
S2	3	(rising adj edge adj flank)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/05/11 11:10
S3	181	(rising adj (edge or flank)) and (falling adj (edge or flank)) and (clock adj buffer adj circuit)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/05/11 11:42
S4	31	(rising adj (edge or flank)) and (falling adj (edge or flank)) and ((clock adj buffer adj circuit) with inverter)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/05/11 11:12
S5	4	S4 and (driving with load)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/05/11 11:27
S6	2	S5 and (gate with width)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/05/11 11:15
S7	2851	inverter and (gate adj width)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/05/11 11:42
S8	5	S7 and (driving with load with edge)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/05/11 11:28
S9	508	inverter with (gate adj width)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/05/11 11:42

S10	1	S9 and (rising adj (edge or flank)) and (falling adj (edge or flank)) and (clock adj buffer adj circuit)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/05/11 11:44
S11	47	S9 and (gate adj width) with larger with inverter	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/05/11 11:45
S12	3	(US-20020191037-$).did. or (US-6344816-$ or US-6717604-$). did.	US-PGPUB; USPAT	OR	ON	2005/05/28 16:07
S13	0	S12 and (clock with buffer) and inverter and (rising with edge) and (gate adj width)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/05/28 16:10
S14	1	S12 and (clock with buffer) and inverter and (rising with edge)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/05/28 16:11
S15	1	S14 and NAND	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/05/28 16:12
S16	0	S15 and (gate with width)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/05/28 16:11
S17	943	clock with buffer with circuit with inverter	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/25 16:26
S18	317	S17 and synchronization	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/25 16:18
S19	5	S18 and (clock adj synchronous adj circuit)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/25 16:22

S20	3	S19 and ((front or leading) adj edge)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/25 16:28
S21	533	(clock adj buffer adj circuits)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/25 16:26
S22	54	(clock adj buffer adj circuits) with inverter	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/25 16:28
S23	1	S22 and ((first adj transistor) and synchronization)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/25 16:27
S24	3	S22 and ((front or leading) adj edge)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/25 16:34
S25	2	S22 and (inverter with (first adj transistor) and (second adj transistor))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/07/11 08:31
S26	1	S22 and (inverter with ((first with transistor) and (second with transistor)) with synchronization)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/25 16:37
S27	3	S22 and (inverter with ((first with transistor) and (second with transistor)))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/25 16:40
S28	3	S27 and edge	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/25 16:40
S29	0	S27 and ((leading or front) adj edge)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/25 16:40

S30	2108	CMOS and (gate with width with (different or larger or smaller or narrower))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/07/05 12:51
S31	26	S30 and (inverter with (clock with buffer))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/07/05 13:18
S32	14	S31 and (edge with (leading or front or trailing or back or rising))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/07/05 13:02
S33	9	S32 and (inverter with gate with width)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/07/11 08:34
S34	54	(clock adj buffer adj circuits) with inverter	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/07/11 08:34
S35	3	S34 and (inverter with ((first with transistor) and (second with transistor)))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/07/11 08:34
S36	1	S35 and (inverter with gate with width)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/07/11 08:35